SPECIFICATION AMENDMENTS

Amendments to the paragraph beginning at page 2, line 5:

Now, a method of manufacturing the BiCMOS semiconductor device in the prior art will be described with reference to Figs. 6(a)-6(c) and 7(a)-7(c).

Amendments to the paragraph beginning at page 2, line 15:

Then, as shown in Fig. 6(b), the lower layer poly-silicon electrode film 10 is formed on the entire surface of the substrate by low pressure CVD ~~process~~ after selectively forming the p-type base layer 8 by photolithography ~~process~~ and ion implantation ~~process~~. Then, the lower layer poly-silicon electrode film 10 and the gate insulating oxide film 7 are selectively etched using a resist formed by photolithography ~~process, then~~ and arsenic is implanted by ion implantation ~~process~~, whereby the n-type emitter layer 9 is formed.

Amendments to the paragraph beginning at page 2, line 24:

Then, washing or cleaning of organic residue ~~away~~ from the resist and so on used in the photolithography process, is carried out prior to the formation of the upper layer poly-silicon electrode film 11. A series of cleaning ~~process~~ processes is shown in Fig. 8. In the final deionized-water rinsing step (S9) and in the drying (IPA vapor drying, spin drying or warm air drying) step (S10) in the cleaning process, it sometimes happens that a natural oxidation film 30 grows with a locally large variation in thickness. The natural oxidation film grows due to a surface oxidation reaction in the chemical processing step and/or reaction of water remaining due to insufficient drying in the drying step.

Amendments to the paragraph beginning at page 3, line 6:

Then, as shown in Fig. 6(c), ~~the~~ arsenic ~~ion is~~ ions are implanted in the entire surface of the upper layer poly-silicon electrode film 11 after forming the upper layer poly-silicon electrode film 11 by low pressure CVD ~~process~~, and then, the arsenic ~~ion~~ ions implanted in the upper layer poly-silicon electrode film 11 ~~is~~ are activated by heat treatment at about 800°C to 900°C and diffused into the lower layer poly-silicon electrode film 10, so that the resistance between the upper layer poly-silicon electrode film 11 and the lower layer poly-silicon electrode film 10 is reduced.

Amendments to the paragraph beginning at page 3, line 16:

Then, as shown in Fig. 7(a), the electrode film 12 of ~~Wsi~~ WSi, being one of the low resistant high refractory ~~metals~~ metal compounds, is formed by ~~spattering method~~ sputtering. Subsequently, the WSi electrode film 12, the upper layer poly-silicon electrode film 11, and the lower layer poly-silicon electrode film 10, of which the resistance has been reduced, are selectively etched by photolithography ~~process~~ and etching, so that a bi-polar emitter electrode and a MOS gate electrode are formed.

Amendments to the paragraph beginning at page 3, line 24:

Then, as shown in Fig. 7(b), the p-type source/drain diffused layer 13 and the n-type source/drain diffused layer 14 are selectively formed by photolithography ~~process~~ and ion implantation ~~process~~.

Amendments to the paragraph beginning at page 3, line 28:

Then, as shown in Fig. 7(c), after forming the interlayer insulation film 15 composed of a BPSG film or the like on the entire surface of the substrate, a contact hole is formed by photolithography ~~process~~ and etching. Then, the metallic electrode film 16 composed of an AlSiCu film or the like is formed, and finally the final passivation film 17 composed of a p-SiN film or the like is formed. The conventional semiconductor device is manufactured through the above-described process.

Amendments to the paragraph beginning at page 4, line 13:

In the final deionized-water rinsing step (S9) and the drying step (S10) of the cleaning process employed prior to the formation of the upper layer poly-silicon electrode film 11, a natural oxidation film 30 in the ~~shape~~ form of a stain, referred to as a water-mark, may grow with a locally wide variation in thickness on the surface of the silicon wafer, resulting from a naturally drying water drop ~~stuck~~ on the surface during or after the drying step. However, as the phenomenon of water drop adhesion is a phenomenon depending upon probability, the natural oxidation film 30 is formed, in some cases, on the interface between the n-type emitter layer 9 and the upper layer poly-silicon electrode film 11 as shown in Fig. 9(a), while in some other cases, not formed as shown in Fig. 9(b). In the connection between the n-type

emitter layer 9 and the upper layer poly-silicon electrode film 11, it is ideal that the natural oxidation film 30 is not formed and the contact resistance is low as shown Fig. 9(b). However, in actual ~~process~~ practice, as shown in Fig. 9(a), the natural oxidation film 30 with large variation in local thickness is usually formed on the interface between the n-type emitter layer 9 and the upper layer poly-silicon electrode film 11, whereby variation in contact resistance occurs. Moreover, in the BiCMOS portion, as the arsenic ~~ion~~ ions implanted in the upper layer poly-silicon electrode film 11 through the natural oxidation film 30 with the wide variation of local thickness ~~thereof is~~ are diffused in the lower layer poly-silicon electrode film 10, the state of diffusion of the arsenic ~~ion~~ ions varies from place to place in the lower layer poly-silicon electrode film 10. As a result, a problem exists in that something abnormal takes place in device characteristics.

Amendments to the paragraph beginning at page 8, line 11:

Figs. 2(a)-2(c) are cross sectional views each showing a manufacturing process of the semiconductor device according to Embodiment 1 of the invention.

Amendments to the paragraph beginning at page 8, line 14:

Figs. 3(a)-3(c) are cross sectional views each showing a manufacturing process of the semiconductor device according to Embodiment 1 of the invention.

Amendments to the paragraph beginning at page 8, line 22:

Figs. 6(a)-6(c) are cross sectional views each showing a manufacturing process of the semiconductor device according to the prior art.

Amendments to the paragraph beginning at page 8, line 25:

Figs. 7(a)-7(c) are cross sectional views each showing a manufacturing process of the semiconductor device according to the prior art.

Amendments to the paragraph beginning at page 9, line 1:

Figs. 9(a)-9(c) are views to explain problems incidental to the semiconductor device

according to prior art.

Amendments to the paragraph beginning at page 9, line 10:

Fig. 1 is a cross sectional view showing a semiconductor device according to Embodiment 1 of the invention. ~~Fig.~~Figs. 2(a)-2(c) and 3(a)-3(c) are cross sectional views showing a manufacturing process of the semiconductor device according to Embodiment 1 of the invention.